REMARKS/ARGUMENTS

Favorable reconsideration of this application in light of the following discussion is respectfully requested.

Claims 21-40 remain active in this application.

In the outstanding Office Action, the amendment filed August 8, 2005 was objected to under 35 USC 32(a) as introducing new matter into the disclosure; Claims 21-32 were rejected under 35 U.S.C. §112, second paragraph, as being indefinite; and Claims 33-40 were rejected under 35 U.S.C. §102(e) as being anticipated by Imamiya et al. (U.S. Patent No. 6,741,499, hereinafter called "Imamiya").

Applicants respectfully traverse the outstanding grounds for rejection of Claims 21-32 under 35 U.S.C. §§ 1323(a) and 112, second paragraph, as being indefinite, because in Applicants' view the claimed subject matter is clearly disclosed in the original specification. In that regard, it is noted that the specification and the drawings clearly disclose first, second and third addresses. For example, as is evident from FIG. 2, the first address corresponds to "n bit data" output from fuse circuits F0 and F1. The second address corresponds to "n bit data" output from data latch circuit 26. The third address corresponds to "n bit data" output from address buffer 11. Accordingly, it is respectfully submitted that the outstanding grounds for rejection of Claims 21-32 under 35 U.S.C. §§ 132(a) and 112, second paragraph, are in error and are traversed.

As there were no other grounds for rejection of Claims 21-32, these claims are believed to be in condition for formal allowance.

Turning now to the rejection on the merits of Claims 33-40, Applicants likewise respectfully traverse this rejection as based on an erroneous reading of the prior art.

More particularly, pending independent Claim 33 defines the subject invention as follows:

Claim 33 A method of testing a redundancy fuse circuit, comprising:
latching a defective address to a data latch circuit;
comparing an input address from a tester with the defective address;
replacing a defective cell with a redundancy cell when the input address is coincident with the defective address;
executing a test on the redundancy cell; and
programming the defective address to a fuse circuit after the test.

The outstanding Official Action relies on Imamiya at column 1, lines 22 - 27 as disclosing that a defective address is stored in a laser-programming type fuse circuit. However, as stated in Claim 33, the defective address is latched to a latch circuit. The invention of Claim 33 therefore differs from Imamiya. In addition, it is well known to the person skilled in the art that a latch circuit and a fuse circuit are completely different circuits.

As for the step of comparing an input address and a defective address, the outstanding Official Action refers to Imamiya at column 1, lines 27 – 50 as disclosing that the input address is compared with a defective address from a fuse circuit. However, it is respectfully submitted that Imamiya does not at all disclose that the input address is compared with a defective address from a latch circuit.

As for the step of testing a redundancy cell, the outstanding Official Action refers to Imamiya, at column 1, lines 35 - 48 as disclosing that a memory cell array is tested for finding a defective address. However, it is respectfully submitted that Imamiya does not at all disclose that the redundancy cell itself is tested.

Finally, as for the step of storing a defective address in a fuse circuit after the test on a redundancy cell, the outstanding Official Action refers to Imamiya at column 1, lines 45 – 46 as teaching this feature. However, it is respectfully submitted that the cited passage discloses nothing relevant to the step of storing a defective address in a fuse circuit after the test on a redundancy cell. On the contrary, Imamiya only discloses a general technique that a defective address is stored in a fuse circuit after the test on a memory cell array.

In view of the above-identified deficiencies in the Imamiya reference, it is respectfully submitted that Claims 33 - 40 are clearly not anticipated by Imamiya and that the

outstanding rejection on that basis is traversed. The rejection of Claims 33-40 under 35 U.S.C. § 102(e) is therefore believed to have been overcome and Claims 33-40 are likewise believed to be in condition for allowance..

Accordingly, no further issues are believed to be outstanding, and it is respectfully submitted that claims 21-40 are in condition for formal allowance. An early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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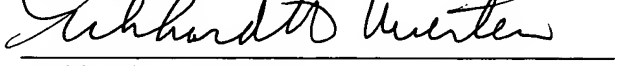

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